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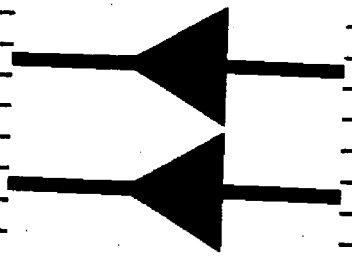

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Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies

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ABSTRACT - The first integrated circuit to economically combine a 700 volt, 3 Ω, high-speed power MOSFET switch with a full-function current programmed pulse width modulation control circuit is introduced. 60 watt 220 VAC input and 30 watt universal input flyback power supply designs are described.

I. INTRODUCTION

The power supply industry continues to push for higher power densities and the power components industry is responding in many ways. Passive components are adapting to the requirements of higher frequency and higher efficiency designs. Active component manufacturers are responding by producing parts with higher levels of integration to support these designs. For example, the PWR-SMP260 combines an 700 V, 3 Ω MOSFET, a fully featured current-mode controller, and an extended set of circuit and load protection features.

Digital synthesis is used in the protection features to eliminate many analog problems encountered in long time delays. This design has eliminated the need for large value, low leakage timing capacitors required for "latched" fault logic and "full cycle" soft start functions in other designs [1]. The integration of the logic-level MOSFET with the current-mode controller has allowed optimization of the gate drive design. It also allows the entire delay time from current-mode comparator to MOSFET output to be guaranteed without performance assumptions of an external gate driver.

Minimum external parts count is a goal for all high-density designs. The PWR-SMP260 requires seven external components including the off-line and bootstrap bias supplies. The integrated circuit is designed to connect directly to an optical coupler without any primary-side support circuitry.

Wide range bootstrap and off-line bias supplies make the integrated circuit ideal for universal input battery charging applications as well as power supply applications. The feature set required for battery charging applications contains all of the power supply requirements plus additional requirements. Battery chargers require a wide range output voltage, precise control of the output power, and a method of turning the charger on and off.

II. FUNCTIONAL DESCRIPTION

The integrated circuit combines a 700 V, 3 Ω MOSFET with a high speed current mode control circuit, high voltage off-line and bootstrap linear regulators, and power supply fault detection and recovery sequencing circuits. The block diagram is partitioned into two sections. The current mode control circuit and power MOSFET is shown in Figure 1 and the high voltage linear regulators and power supply fault detection and recovery sequencing circuits are shown in Figure 2.

A. The Power MOSFET

The gate drive requirements are significantly reduced because of the logic-level threshold voltage and very low Miller capacitance of the lateral geometry MOSFET. However, in an integrated solution the advantage of these characteristics is apparent to the user only as low bias supply current. The power supply designer need only be concerned with the output terminal characteristics of the MOSFET.

The conduction losses of the output MOSFET can be calculated from the on-state resistance ($R_{DS(ON)}$). $R_{DS(ON)}$ is 3 Ω for currents up to 1 A, and increases to 4 Ω at greater than 2 A. The practical limit for peak drain current in continuous operation is greater than 2 A. Switching losses due to the stored charge on the drain can be calculated from the 4.5 μJ of stored energy at 400 V. The stored charge in the output rectifier and transformer capacitance must be taken into account to get a good estimate of the total switching loss.

B. The Current Mode Controller

Many of the discrete components required in a current-mode controller design have been integrated in the summing junction function. The number of support components required for a production design has been reduced by at least a factor of two as compared to a "3842/3823 style" circuit.

1) *Summing Junction:* The output of the summing junction is a current source. The constant current flowing through R_C creates a fixed offset voltage. The current mode controller compares this offset voltage to the voltage across the primary current sense resistor R_s. The full scale summing junction output current (480 μA) times the ratio of the gain setting resistor R_C to the current sense resistor R_s will set the maximum current for the current mode controller and output MOSFET. If the

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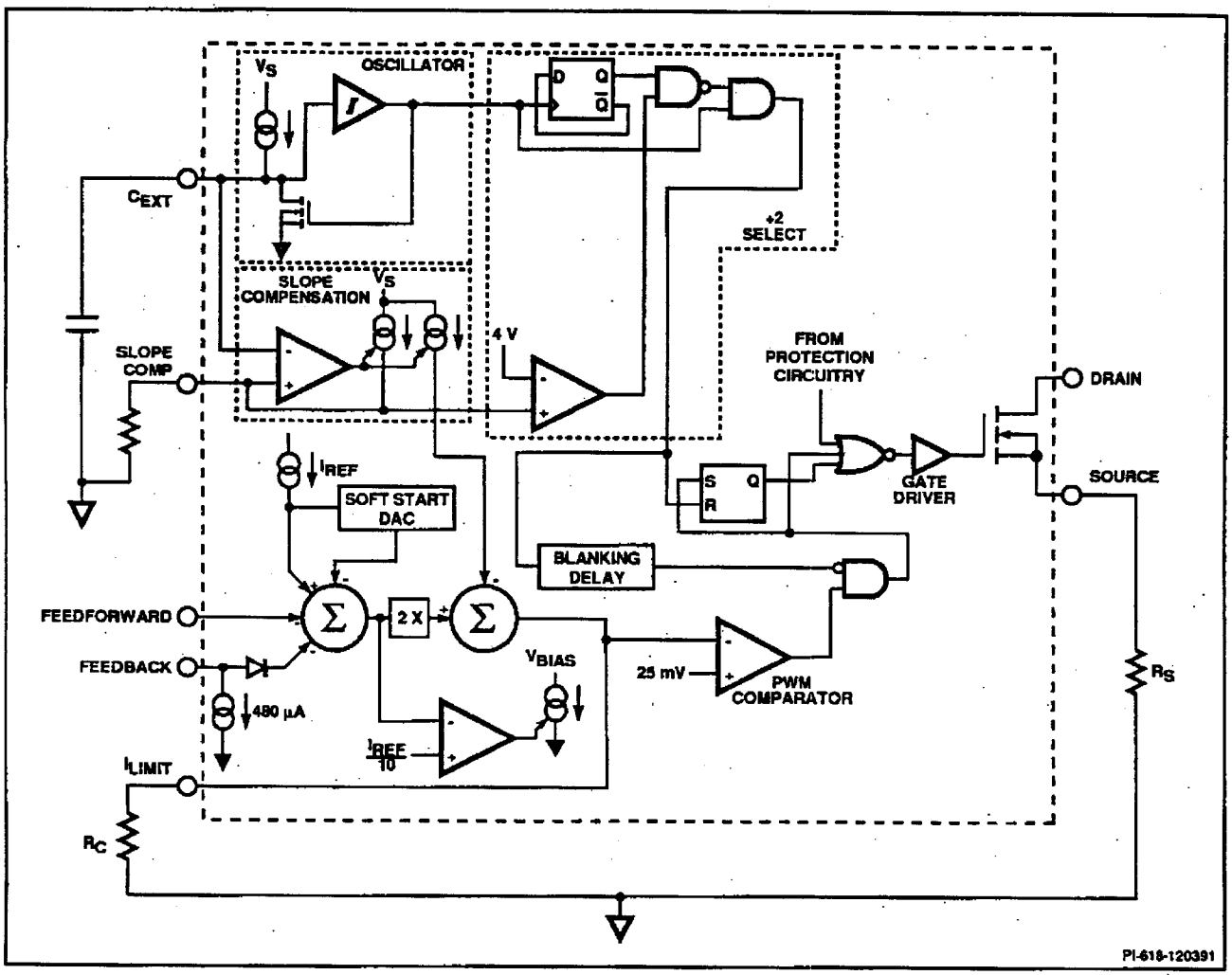

Figure 1. Detailed block diagram of the control and power output sections of the PWR-SMP260.

current sense resistor is 0.25 Ω and the maximum desired switch current is 2 A, then the gain setting resistor R_c should be

$$0.25\Omega \times \left(\frac{2A}{0.48mA}\right) = 1k\Omega. \qquad (1)$$

The output of the summing junction can be controlled by injecting a current into the feed forward pin or the optical coupler pin. Current flowing into these pins will linearly decrease the current flowing from the summing junction output and correspondingly the peak current in the output switch. The optical coupler input pin has a current source associated with it. The current source insures that the optical coupler will be biased at 0.48 mA before the summing junction output current will be affected [2]. The voltage on these pins are 1.25 and 2 V respectively and have input impedances of less than 1 kΩ. The feedforward and optical coupler currents have a gain of 2 within the summing junction.

The part is designed for a secondary-referenced error amplifier with optical feedback. However, primary side regulation can be achieved by adding a primary-referenced error amplifier circuit. A simple error amplifier can be implemented by connecting a Zener diode between the bootstrap bias supply and the optical coupler pin. The current source on the pin will bias the Zener diode and the diode will control the bootstrap bias voltage that is proportional to the output voltage via the transformer turns ratio.

The feedforward pin can be used for control loop compensation for changes in input voltage. A separate pin is provided so that open loop compensation is available when the secondary regulator control loop is open. A constant input power regulator for wide ranges in input and output voltage can be constructed using this feature. This feature along with a wide bootstrap bias supply range is very useful in battery charging applications.

The summing junction also has internal control inputs from the soft start digital to analog converter and the slope compen-

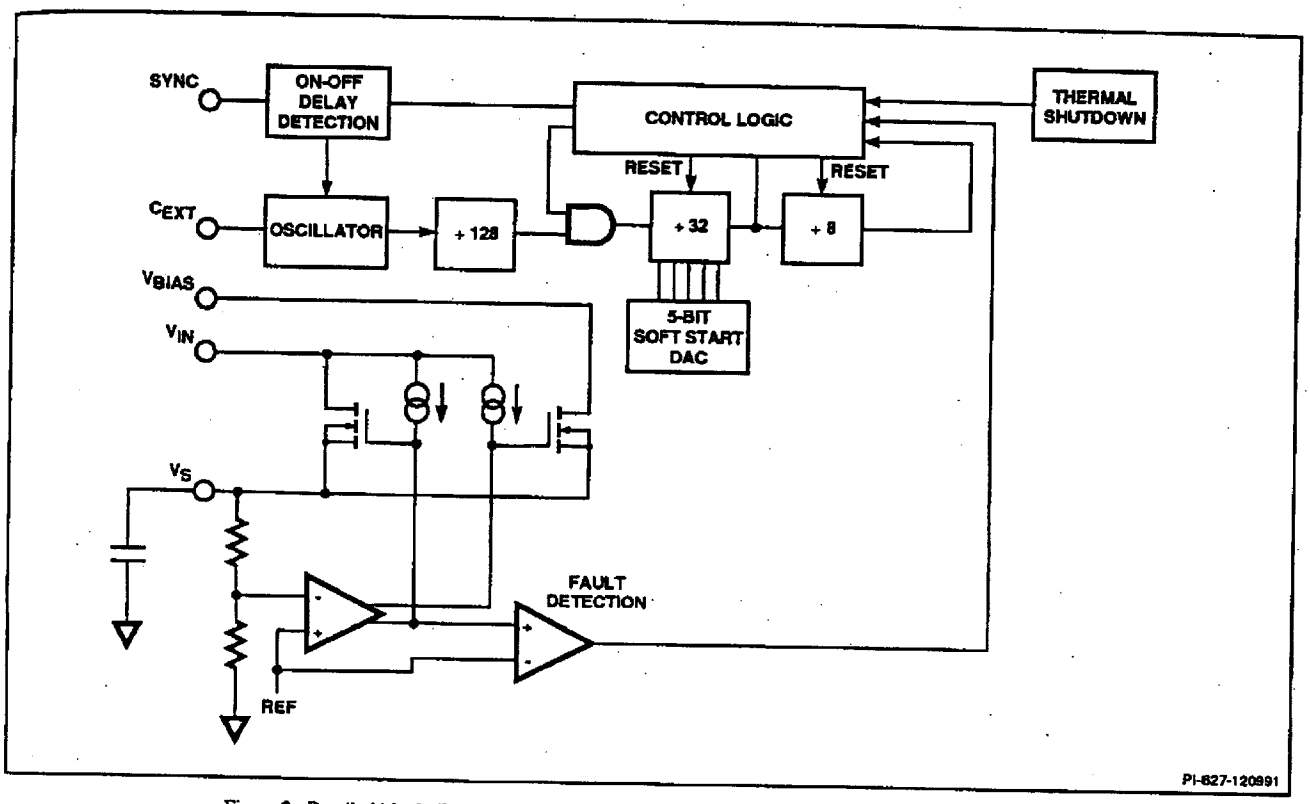

Figure 2. Detailed block diagram of the internal regulator and protection circuitry of the PWR-SMP260.

sation circuit. The soft start digital to analog converter will inject 100% of the reference current into the summing junction at the beginning of the soft start sequence and incrementally decrease the soft start injection to zero.

The slope compensation causes the sum junction output current to be linearly decreased over the programmed pulse width (Figure 3). The rate of decrease is programmable with the slope compensation resistor value. The shape of the compensation current is the same as the oscillator waveform. Slope compensation is inhibited and 50% maximum duty cycle is selected when the slope compensation pin is connected to V_S.

2) *Comparator and Blanking Time:* The key elements of the current-mode control circuit are the comparator, R-S flip flop, gate driver, and output transistor. The two parameters of interest [3] are the delay time from the comparator input to the MOSFET output and the leading edge blanking time. The delay time of current sense comparator, gate driver and output MOSFET are all specified together in an integrated controller. A discrete design must consider the tolerance of each part, also the effect of the printed circuit board layout capacitance and inductance on circuit delay time. Other advantages of an integrated solution are the gate driver is optimized for the output transistor characteristics. An integrated design also removes the chance of noise injection in the critical gate drive printed circuit board layout.

Leading edge blanking allows the turn on current transient to stabilize before the output of the current mode comparator is connected to the R-S flip flop. The start of the blanking time is the turn on of the MOSFET. The blanking time is specified as the maximum time the comparator input can exceed the comparator threshold and recover to 100 mV below the threshold and not have the output MOSFET switch off. The blanking time is designed to allow the turn on current spike to recover in a flyback power supply operating in continuous conduction mode with an "ultra fast" rectifier. A current spike waveform similar to Figure 4 will not cause a circuit malfunction.

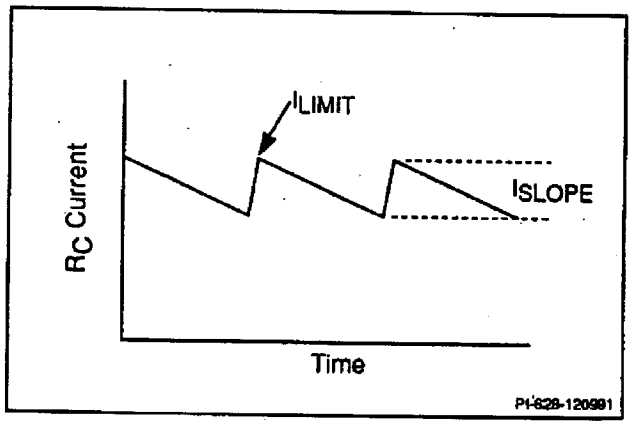

Figure 3. Slope compensation current relationships.

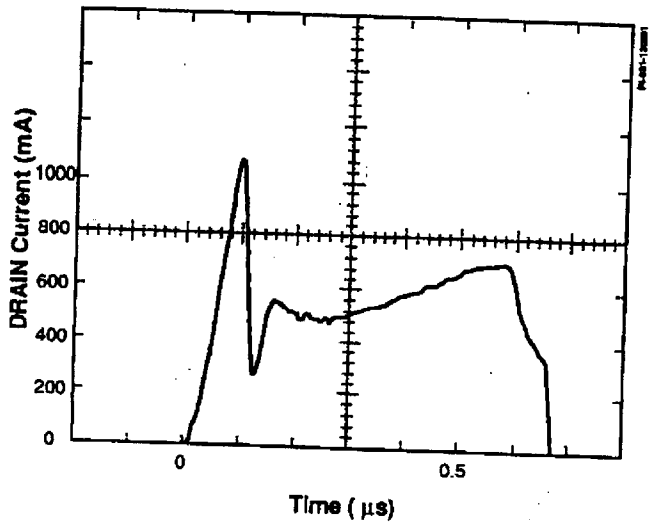

Figure 4. Leading edge current spike example.

3) *Maximum Duty Cycle:* The maximum duty cycle is user programmable. If a 50% maximum duty cycle is desired connect the slope compensation pin to the V_s internal bias supply voltage. A frequency divider flip-flop will be inserted between the oscillator and the current mode R-S flip-flop the maximum duty cycle will be 50%. The oscillator timing capacitor will need adjustment so that the oscillator will run at twice the output frequency.

If a 90% maximum duty cycle is desired connect a resistor between the slope compensation pin and common. The resistor determines the amount of slope compensation current flowing in the output of the summing junction. The slope compensation has the effect of reducing the current flowing from the summing junction linearly with time. Equation (2) shows how to calculate the desired slope compensation resistor value.

$$R_{SLOPE} = \frac{1.75V}{I_{SLOPE}} \qquad (2)$$

A current mode control loop operating in the continuous conduction mode with duty cycles over 50% requires slope compensation for stability [4]. The amount of slope compensation is a function of the slope of the magnetizing current flowing in the MOSFET. Circuits that have discontinuous conduction over the entire duty cycle range do not need slope compensation. However, in noisy environments, a small bypass capacitor is recommended.

4) *Minimum Load:* Current mode control has a well known problem of regulating at minimum load due to minimum pulse width. A minimum width pulse will transfer a incremental amount of power to the output every time the power switch is turned on. Operating at no load usually require compromises that usually take shape as a pre-load resistor on the output or the switching frequency being reduced by initiating a subharmonic oscillation. The pre-load solution is unacceptable in modern thermally limited high efficiency designs. The subharmonic oscillation, often called "hiccup mode" is equally unacceptable because of possible audible noise emissions.

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added (Figure 1). A shunt regulator is activated when the summing junction current falls below 12% of full scale. The shunt regulator will increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale. Figure 5 shows the load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The control loop gain path is shown in Figure 6. The gain of the minimum load regulator has been matched to the gain of the current mode switching regulator. This allows the control loop dynamics remain the same whether the minimum load circuit is active or not active.

The output transient load response is shown in Figure 7. Note that at light load the gain of the switch mode path decreases but the gain of the minimum load path remains the same and the transient load response is not significantly degraded. A interesting side effect of the minimum load circuit is its effect on bias supply power during a transient. The power consumed from the bias supply is greater than the average of the two states when the period of the transient is close to the control loop response time.

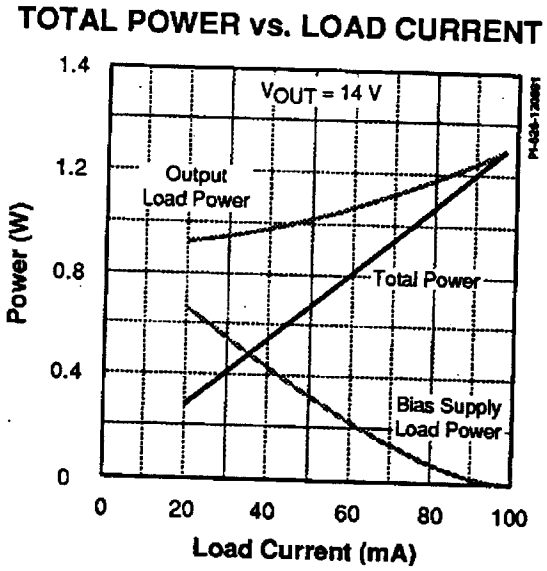

Figure 5. Minimum load transfer effect.

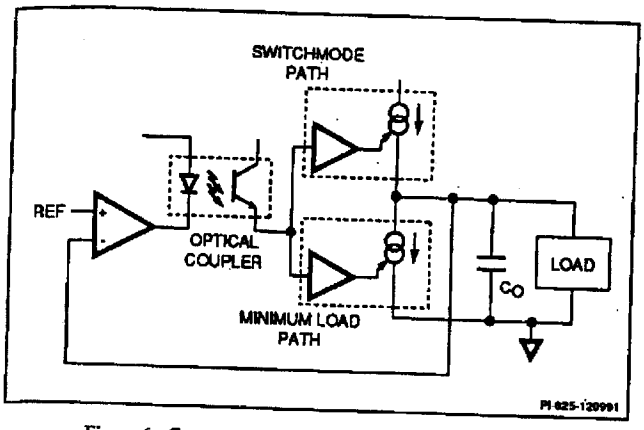

Figure 6. Current mode and minimum load control loop.

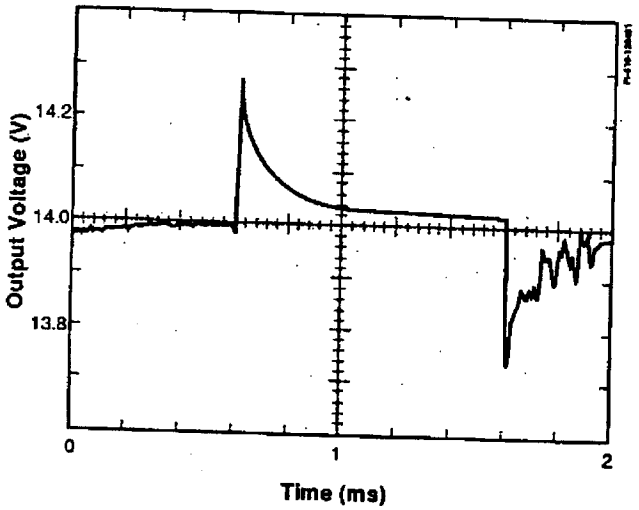

Figure 7. Minimum load output transient response.

The control loop overshoot, settling time and transient repetition rate affect this characteristic. The bias supply load power vs load transient frequency for a 50% duty cycle is shown in Figure 8. The best load transient response occurs when the capacitance on the bias supply is a minimum.

C. Oscillator

The oscillator-switching regulator circuit is designed for optimum performance between 30 and 400 kHz. The oscillator waveform is a sawtooth with a slow rise from zero to 1.75 V followed by a rapid discharge. The oscillator will operate at twice the power supply frequency when the 50% maximum duty cycle option is selected. The oscillator frequency is set with a timing capacitor. The oscillator timing capacitor value can be estimated by dividing 94 µF-Hz by the desired clock frequency.

The oscillator can be synchronized to a clock that is running at a higher frequency. A short pulse of less than 1 µs is applied to the SYNC pin to terminate the clock cycle. The SYNC pin has a CMOS logic level and is negative edge sensitive. However, if the signal is held low for longer than 10 µs, it will be interpreted as an on-off signal sending the circuit into a power down state which continues for as long as the signal is low. The interface circuits for isolated synchronization and ON/OFF signals are shown in Figure 9.

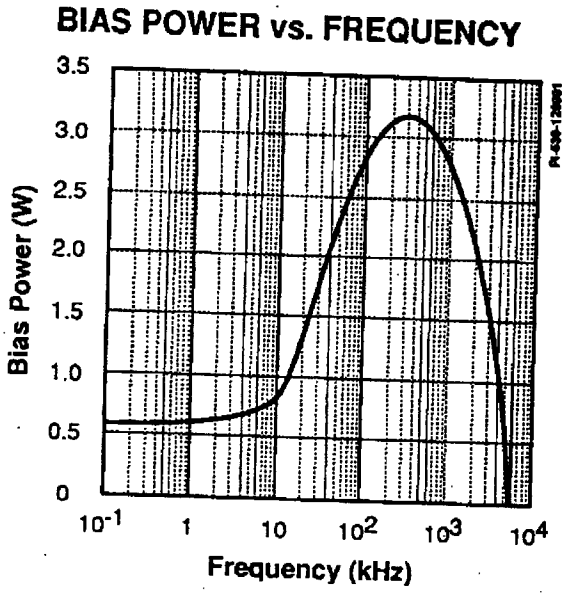

Figure 8. Effect of load transient frequency on bias power.

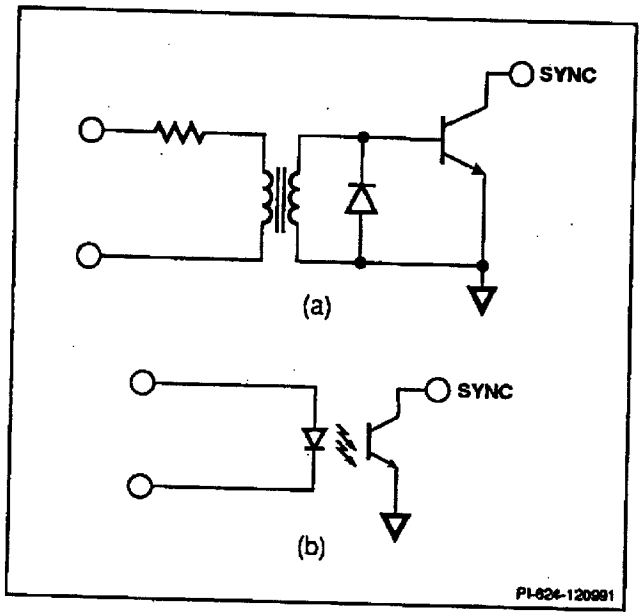

Figure 9. (a) Synchronization and (b) ON/OFF interface circuits.

D. Bias Regulators/Protection Circuitry

The high voltage linear regulators and power supply fault detection and recovery sequencing circuits are shown in the block diagram Figure 2.

1) *Bias Regulators:* The linear regulator for the internal supply voltage V_S has two sources of power. They are the bootstrap bias supply and the off-line high voltage supply. The regulator has a built-in preference for the bootstrap bias supply. Should the bias supply be incapable of supplying the total requirement, the remaining current will be sourced from the off-line voltage. A small current source connected to the V_{IN} pin is the only current consumed from the off-line voltage when the off-line regulator is turned off.

The internal V_S supply voltage will be operational. This occurs at a minimum V_{IN} voltage of 36 V. This is independent of the bootstrap bias supply voltage.

Reverse current through the bootstrap bias regulator transistor has been eliminated. The V_S supply will not be loaded by circuitry powered from the bias supply at turn-on. Additional primary-referenced circuitry may be powered from the bootstrap bias supply without affecting the operation of the control circuit. If reverse current flow were not blocked the V_S could be loaded down and prevent the undervoltage lockout signal from releasing the switch mode regulator.

2) *Protection Functions:* Protection features include input under voltage lockout, over temperature fault, output under voltage fault and output over current protection consistent with cycle by cycle peak limiting of the switch current. The input under voltage lockout holds the gate of the output MOSFET low and resets the soft start counter chain until the V_S supply voltage is within its valid operating range. The fault conditions control the functioning of the "latched fault logic" and restart delay sequence.

The over temperature protection circuit monitors the junction temperature of the power MOSFET and signals a fault when the preset temperature is exceeded. The fault will continue until the junction temperature drops below a lower level. During the time a fault is sensed, the output switching MOSFET is turned off and the soft start counter chain is reset. The power consumption of the control circuit is reduced during a fault to limit self heating of the off-line regulator.

A fault condition also will be declared when the bootstrap bias voltage drops low enough to draw current from the off-line regulator. This condition indicates that the output voltage is significantly out of regulation and an overload condition exists. The fault condition is not declared when the bootstrap bias voltage is low and the minimum load circuit is active. The bootstrap bias voltage can be momentarily be pulled low during a minimum load transient which would erroneously indicate a fault.

The "latched fault logic" turns off the output MOSFET, reduces the power consumption of the control circuit and starts the restart delay sequence. When the counter reaches 28,672 power supply equivalent cycles the soft start sequence starts.

The power up sequence is between 3969 and 4096 power supply equivalent cycles long. During this time the switching regulator circuits are enabled and the bootstrap bias supply should reach its valid operating range. The bootstrap bias voltage is monitored at the end of this period. If the voltage is below the regulation voltage, a fault is signaled and the cycle repeats. This characteristic produces a foldback current limit function as shown in Figure 10. This function is very effective for limiting the dissipation in over load and short circuit conditions.

3) *Soft Start:* During power up the circuit has an optional soft start function. Soft start is enabled by connecting the soft start pin to the V_S pin and disabled by connecting it to common. When soft start is disabled, the maximum switch current is available for power transfer to the output. When the output voltage is low this usually puts the transformer deep into continuous conduction mode. The circulating current rises rapidly and the transformer core can be driven into saturation. The output rectifier also experiences a large current and thermal transient.

When soft start is enabled the maximum output switch current is programmed linearly increasing from zero to maximum in 4096 power supply equivalent clock cycles. A 5 bit digital-to-analog converter controls the current available from the summing junction during the power up period.

Power up is the time when most power supplies fail. The soft start function reduces all of the power supply component peak stresses during the power up sequence. This should produce a power supply with a superior demonstrated reliability.

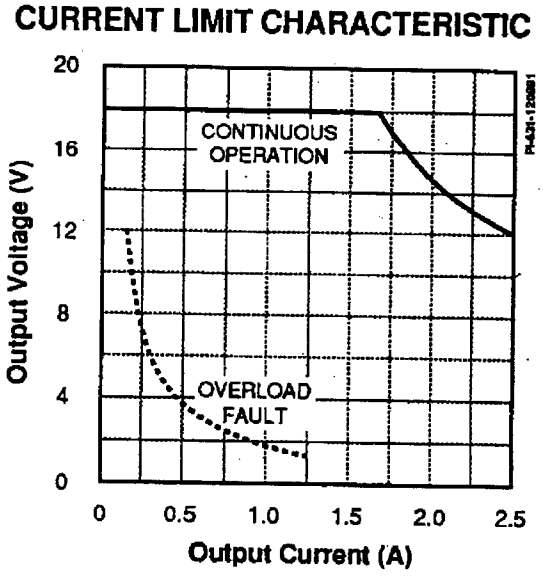

Figure 10. Foldback current limit for flyback operation.

III. CONTROL LOOP MODEL

The current mode control loop can be modeled as a controlled current source driving the total output capacitance of the power supply as shown in Figure 6. The transfer function will have a one pole response and have 90 degrees of phase margin [5].

The gain of the optical coupler is equal to the current transfer ratio (CTR). The CTR for a 4N26 optical coupler is typically 0.5 with a range of 0.3 to 1 when operating at output currents between 0.5 to 0.75 mA[6]. The input impedance of the optical coupler port on the integrated circuit is kept low so that the pole formed by the optical coupler capacitance will be as high frequency as possible.

Equation (3) describes the output voltage to LED current gain of the typical TL431 error amplifier circuits shown in Figures 11 and 12.

$$\frac{I_{LED}}{V_O} = \frac{1 + \left[\left(\frac{1}{2\pi \times R_6 \times C_1}\right) \times \left(1 + \frac{f}{\left(\frac{1}{2\pi \times R_2 \times C_1}\right)}\right)\right]}{R_1} \quad (3)$$

The error amplifier has two forward gain paths. The first is through the amplifier section, which is dominant until the amplifier reaches unity gain. The second is directly from the output to the optical coupler. At frequencies greater than the unity gain frequency the signal path directly from the output to the optical coupler dominates.

Circuits that have an output π filter should partition the error amplifier. The optical coupler should be connected to the input of the π filter and the voltage sensing divider can be connected to the output of the π filter. This insures that the two poles of the output π filter will not be present in the high frequency response of the error amplifier [7].

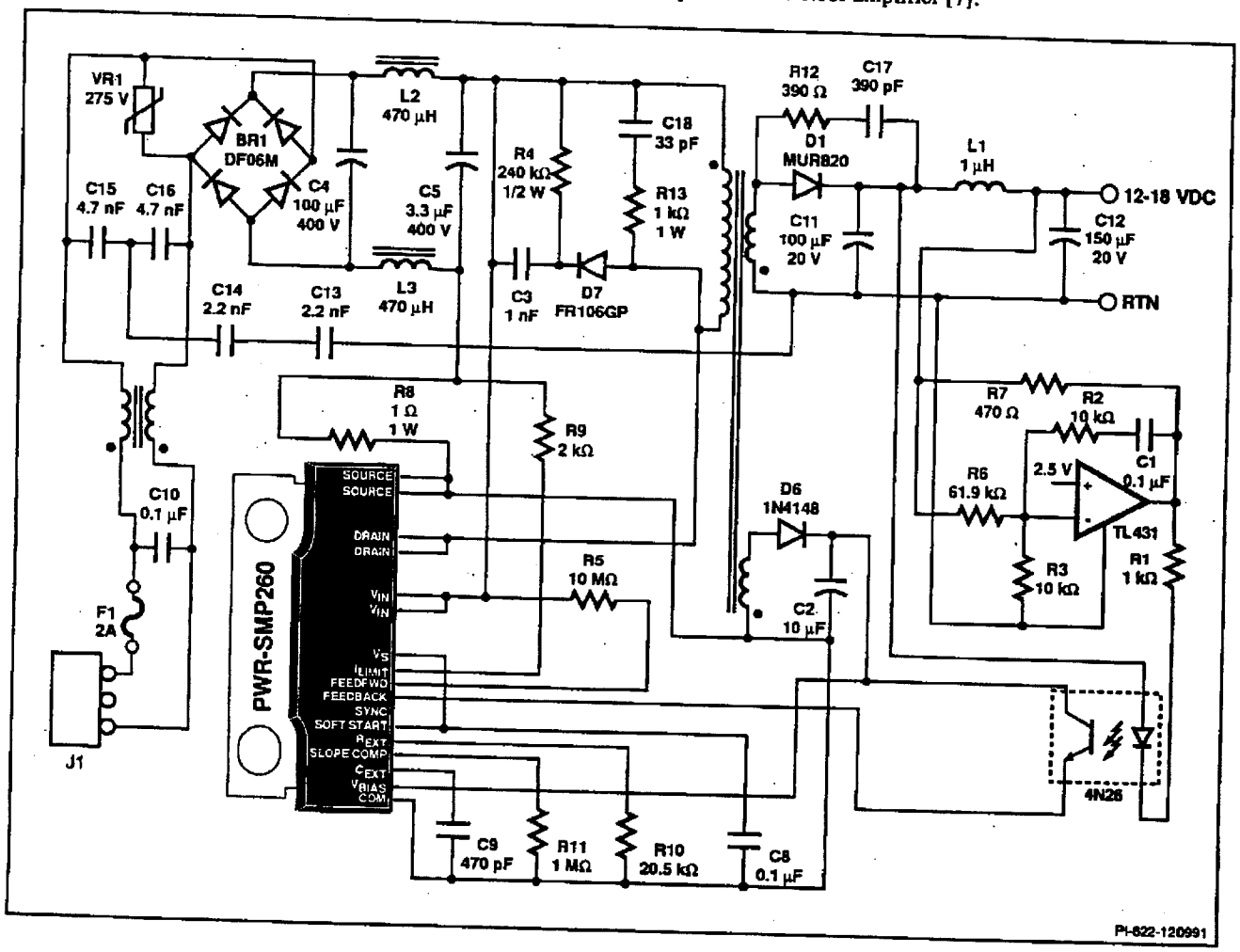

Figure 11. Flyback converter circuit using the PWR-SMP260.

IV. PACKAGE AND LAYOUT CONSIDERATIONS

The integrated circuit package is a single in-line power tab package 30 mm wide by 3.5 mm thick by 20.2 mm high. The high-voltage pins have a 3.1 mm gap between them for international safety spacing requirements. The pins are on 1.27 mm centers with a 2.54 mm stagger bend. This allows a printed circuit board to be designed with a high voltage pad to pad spacing greater than the required 2.5 mm for IEC950. A pad diameter of 1.52 mm and a hole size of 1.02 mm can be used.

The power tab is electrically connected to the source of the output MOSFET. An insulator between the heat sink and the power tab is not required. Connecting the heat sink to the circuit common is also advantageous for EMI suppression.

V. FEATURES APPLIED TO POWER SUPPLY AND BATTERY CHARGING APPLICATIONS

The wide range in bootstrap bias supply voltage 8 to 30 V relieves the granularity of the output to bias winding turns ratio. Battery charging applications require a wide range output voltage to track the terminal voltage of a charging battery.

The bootstrap bias supply under voltage shutdown can prevent a discharged battery with a shorted cell from being charged. The shorted cell will drop the battery terminal voltage below the minimum output voltage and this function will prevent over heating and possible rupture of the remaining cells.

The electronic on/off is also useful in system applications such as battery chargers controlled by microcontrollers. The synchronizing and on/off control pin can be driven using a transformer or optical coupler as shown in Figure 9.

The 90% duty cycle option allows applications to operate down to lower input voltages with some compromise in output ripple voltage and rectifier stress. Built-in slope compensation reduces the external circuitry required to implement this function.

Minimum load control prevents leading edge blanking from requiring a minimum output power. Feedforward control allows for open loop compensation for variations in the input voltage. A design with the correct transformer inductance and operating frequency will provide an open loop constant power transfer circuit. The shutdown automatic restart function requires that the bootstrap bias supply be above 8 V within 4096 equivalent clock cycles. This puts a limit on the amount of capacitance that can be charged during this time.

VI. THE 60 WATT POWER SUPPLY

The schematic for the flyback power supply is shown in Figure 11. The Line and Load Regulation is <0.1%. The same circuit can be designed to operate continuously over the universal input voltage range of 85 to 265 VAC_{RMS} by changing the transformer turns ratio. However, the increase in input voltage range reduces the output power to 30 W. The line, load regulation is <0.1%. The 30 W circuit has been demonstrated within an enclosure with dimensions of 32.5 x 60 x 95 mm.

A forward converter can be constructed by replacing the secondary-side components of Figure 11 with those shown in Figure 12. The output inductor is common with the bias supply to insure minimum load operation.

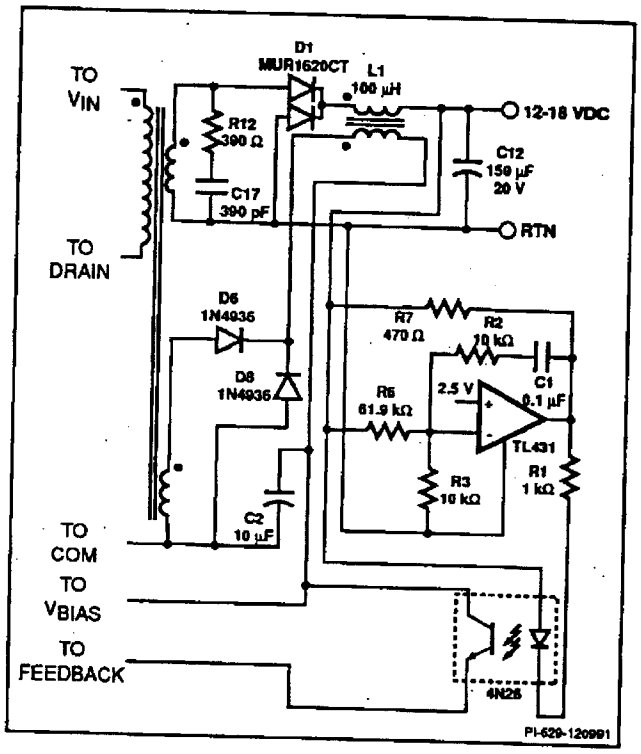

Figure 12. Modifications to the secondary-side circuitry to form a forward converter.

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